FIN-TYPE ANTIFUSE

## DESCRIPTION

[Para 1] BACKGROUND OF THE INVENTION

[Para 2] Field of the Invention

[Para 3] The invention generally relates to a method of forming an antifuse and the resulting structure which includes a fin structure that can be converted from an insulator into a permanent conductor through a heating process.

[Para 4] Description of the Related Art

[Para 5] Fuses and antifuses are useful in today's integrated circuit devices to selectively connect and disconnect devices from other portions of the circuit, as well as to provide logical operations. For example, a fuse is often activated (blown, opened, etc.) in order to disrupt or break an electrical connection. Similarly, a fuse can be blown to dramatically increase the resistance of a circuit, thereby providing a logical distinction between the activated and unactivated fuse device.

[Para 6] Antifuses operate in an opposite manner to that of fuses. Thus, antifuses are generally non-conductive (highly resistive) when unactivated (unblown) and become conductors when activated (blown). Therefore, when an antifuse is activated, it forms an electrical connection, as opposed to a fuse which breaks an electrical connection when activated. Thus, an antifuse selectively allows a conductive connection to be made to selectively connect portions of a circuit together, thereby potentially engaging a

previously disconnected device into a circuit. Similarly, an antifuse provides different resistance values which can be utilized to perform logical operations.

[Para 7] Once a fuse or antifuse is activated, the fuse generally cannot be unactivated. Therefore, the activation is generally a one-time event and is used to permanently modify a circuit. Low process cost and relatively high density are required for fuses and antifuses. Electrically blowing metal fuses is one conventional method for activating a fuse, but requires precise electrical and physical control to be reliable. The invention described below provides much smaller and easily activated antifuses and methods for making the same.

[Para 8] SUMMARY OF THE INVENTION

[Para 9] This disclosure presents a method of forming an antifuse and the resulting structure. The invention forms a material layer and then patterns the material layer into a fin. Next, the invention converts the center portion of the fin into a high-resistance conductor and the end portions of the fin into conductors. The process of converting the center portion of the fin into a high-resistance conductor (substantially non-conductive) allows a process of heating the fin above a predetermined temperature to convert the high-resistance conductor into a low-resistance conductor (substantially conductive). Thus, the invention provides a fin-type structure that can be selectively converted from a high-resistance conductor into a low-resistance conductor using a simple heating process.

[Para 10] In the process of converting the center portion of the fin into a high-resistance conductor, the ends of the fin are masked such that the center portion of the fin is unprotected, and then ions are implanted into the center portion of the fin. This process changes the center portion of the fin into an amorphous material. Thus, for example, this process of converting the center portion of the fin into a high-resistance conductor changes the center portion from single-crystal silicon to amorphous silicon. The subsequent selective heating of the fin changes the center portion of the fin into polycrystalline

silicon. The selective heating of the fin that activates the antifuse changes the conductivity level of the center portion of the fin to be many times more conductive (e.g., 10 times more conductive) after being heated above the predetermined temperature when compared to the conductivity level of the center portion before heating. In a similar manner, the process of converting the end portions of the fin into conductors can comprise protecting the center portion of the fin, and then siliciding the end portions of the fin.

[Para 11] In another embodiment, the invention forms a directional antifuse that has a preferred direction of condition (bias) before and after being activated. This embodiment again patterns a material layer into a fin. The end portions of the fin are converted into a P-type end and an N-type end and the center portion of the fin is converted into a P-N junction. This process of converting the center portion of the fin into the P-N junction allows a process of heating the fin above a predetermined temperature to permanently change characteristics of the P-N junction.

[Para 12] More specifically, the process of converting the center portion of the fin into a P-N junction comprises masking ends of the fin such that the center portion of the fin is unprotected. Then ions are implanted into the center portion of the fin. The process of implanting ions into the center portion of the fin changes the center portion of the fin into an amorphous material. The process of converting the end portions of the fin into conductors comprises protecting the center portion of the fin, protecting the N-type end and implanting P-type impurities into the P-type end, and protecting the P-type end and implanting N-type impurities into the N-type end. These N-type impurities and the P-type impurities comprise opposite type impurities. After the P-type and N-type impurities are implanted into the ends of the fin, the fin is heated sufficiently to drive impurities from the ends of the fin into the center of the fin.

[Para 13] The heating of the fin decreases the density of mid-gap states of the center portion of the fin by, typically two to three orders of magnitude, compared to the level of the center portion before heating. Thus currents

across the P-N junction when reverse biased are decreased by two or more orders of magnitude (e.g., suppress by 100X or more) after heating.

[Para 14] One of the antifuse structures provided by the invention comprises a fin having a center portion and end portions. The center portion of the fin comprises an insulator adapted to permanently become a conductor when heated above a predetermined temperature and the end portions comprise permanent conductors.

[Para 15] In this structure, the center portion of the fin comprises an amorphous material that is many times more conductive after being heated above the predetermined temperature when compared to a conductivity level of the center portion before heating. For example, the center portion can comprise single crystal silicon before being heated above the predetermined temperature and is changed to polycrystalline silicon after being heated above the predetermined temperature. The end portions comprise a permanent conductor, such as silicide regions of the fins.

[Para 16] The size (length) of the center portion of the fin is restricted such that, for example, the center portion comprises a very small portion (less than approximately 10 percent) of the length of the fin. Further, the fin is a rectangular structure that extends from a substrate and is more than a conventional rectangular wire. Thus, for example, the fin has a height and length that exceeds more than many times (e.g., 2 or more times) the width of the fin.

[Para 17] In the embodiment of the antifuse that has a bias (similar to a diode), the center portion of the fin comprises a P-N junction adapted to permanently change characteristics when heated above a predetermined temperature and the end portions comprise a P-type end and an N-type end. Again in this embodiment, the center portion of the fin can comprises an amorphous material, which can comprise, for example, single crystal silicon before being heated above the predetermined temperature and polycrystalline silicon after being heated above the predetermined temperature.

[Para 18] These and other aspects of embodiments of the invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the embodiments of the invention without departing from the spirit thereof, and the invention includes all such modifications.

[Para 19] BRIEF DESCRIPTION OF THE DRAWINGS

[Para 20] The embodiments of the invention will be better understood from the following detailed description with reference to the drawings, in which:

[Para 21] Figure 1 is a schematic diagram of a partially completed antifuse according to the invention;

[Para 22] Figure 2 is a schematic diagram of a partially completed antifuse according to the invention;

[Para 23] Figure 3 is a schematic diagram of a partially completed antifuse according to the invention;

[Para 24] Figure 4 is a schematic diagram of a partially completed antifuse according to the invention;

[Para 25] Figure 5 is a schematic diagram of a partially completed antifuse according to the invention;

[Para 26] Figure 6 is a schematic diagram of a completed antifuse according to the invention;

[Para 27] Figure 7 is a schematic diagram of a partially completed antifuse according to the invention;

[Para 28] Figure 8 is a schematic diagram of a partially completed antifuse according to the invention;

[Para 29] Figure 9 is a schematic diagram of a partially completed antifuse according to the invention;

[Para 30] Figure 10 is a schematic diagram of a completed antifuse according to the invention;

[Para 31] Figure 11 is a schematic diagram of inventive antifuse used within a circuit; and

[Para 32] Figure 12 is a flow diagram illustrating the inventive methodology.

[Para 33] DETAILED DESCRIPTION OF PREFERRED

[Para 34] EMBODIMENTS OF THE INVENTION

[Para 35] The invention presents a method of forming an antifuse and the resulting structure. The inventive method and structure produce antifuses that use fin technology. Therefore, the inventive antifuses are smaller than conventional fuses. Thus, the invention takes advantage of the fact that a fin of silicon is of very low mass (fractions of a picogram) and thus is easily heated electrically. The invention provides an inexpensive technique to make the antifuse change resistance by a large amount (e.g., 10X) permanently after a pulse of heating current is passed through the fin. Because of the small area (mass) of the inventive structure, the operation of activating (blowing) the antifuse involves a simplified heating process that is performed by passing current through the antifuse. Therefore, not only does the invention produce smaller antifuses than are conventionally available, the invention also provides

a method of activating the antifuses that avoids the problems that can occur during conventional physical/optical antifuse activation.

[Para 36] Figures 1-3 illustrate some non-limiting ways in which the fin structure may be formed. As shown in Figure 1, the invention forms a material layer 102 (such as single crystal silicon, silicon-germanium, etc.) on a substrate 100 (a silicon wafer, a SOI wafer, etc.). A mask 104 (such as an organic photoresist, etc.) is patterned over the material 102 and a common material removal process such as etching, chemical treatment, etc. is used to remove the exposed portion of the material 102 to leave a freestanding fin 200. Note that the fin 200 is a rectangular structure that extends from the substrate 100 and is more than a conventional rectangular wire. Thus, for example, the fin has a height (h) and length (l) that exceeds more than 2 times the width (w) of the fin.

[Para 37] An alternative method to form the fin 200 is shown in Figure 3. This method is sometimes referred to as sidewall spacer technology. In this method, a placeholder 300 is patterned on the substrate 100 using conventional techniques such as photolithography. Then, the material 102 is deposited over the placeholder 300. Next, a selective directional etching process is utilized to remove the material 102 from horizontal surfaces at a higher rate than it removes material from vertical surfaces. This leaves the material 102 only on the side walls of the placeholder 300. The upper surface of the structure is then preferably polished to remove any excess material 102, leaving the fin structure 200 shown in Figure 3. After this, the placeholder 300 is removed resulting in the structure shown in Figure 2.

[Para 38] Figure 4 illustrates the process of converting the center portion of the fin 200 into an insulator. In Figure 4, the previous masks are removed and the ends of the fin are protected using another mask, such as a photoresist 400. The center portion of the fin is left unprotected. Then, high-mass ions 402 (such as silicon, germanium, arsenic, xenon, etc.) are implanted into the center portion of the fin 200. This ion implant 402 is sufficient to make the central portion of the fin 200 and amorphous insulating material.

For example, the ion implant energies can be between approximately 0.5 keV and approximately 3 keV with a normal dosage in the range of $1 \times 10^{14}\,cm^{-2}$ to $5 \times 10^{14}\,cm^{-2}$. Once again, this process changes the center portion of the fin 200 into an amorphous material. Thus, for example, this process of converting the center portion of the fin into an insulator changes the center portion of a silicon fin into a region of amorphous silicon.

[Para 39] In Figure 5, the previous masks are removed and another mask 500, that is similar to the previous masks discussed above, is patterned to protect the center portion of the fin 200 and allow the ends of the fin to be exposed. The exposed portions of the fin are converted into conductors by implanting an impurity in sufficient quantity to make the ends of the fin 200 conductive. Alternatively, the ends of the fins 200 can be silicided 502 in a process that heats the fin in a metal containing ambient. In addition, as would be understood by one ordinarily skilled in the art given this disclosure, many additional methods can be utilized to make the ends of the fin 200 conductive. Then the mask 500 is removed leaving the structure shown in Figure 6 that includes a high-resistance center section 600 and conductive ends 602, 604.

[Para 40] Thus, the invention converts the center portion 600 of the fin into a high-resistance (substantially non-conductive) region and the end portions 602, 604 of the fin into conductors. The process of converting the center portion of the fin into a high-resistance region allows a subsequent process of heating the fin above a predetermined temperature to convert the high-resistance region into a low-resistance region. Thus, the invention provides a fin-type structure that can be selectively converted from a high-resistance conductor into a permanent low-resistance conductor using a simple heating process.

[Para 41] In another embodiment, shown in Figures 7-10, the invention forms a directional antifuse that has a preferred direction of conduction (bias) before and after being activate. This antifuse operates as a P-N junction in a similar manner that a diode operates, except that the activation of the P-N junction within the fin 200 changes the characteristics of the P-N junction

dramatically allowing the antifuse to be easily utilized as a logical device. In this embodiment, the end portions of the fin are converted into a P-type end and an N-type end and the center portion of the fin is converted into a P-N junction. This process of converting the center portion of the fin into the P-N junction allows a process of heating the fin above a predetermined temperature to permanently change characteristics of the P-N junction.

[Para 42] More specifically, as shown in Figure 7, the process of converting the center portion of the fin 200 into a P-N junction comprises masking ends of the fin 200 (again using a mask such as mask 400) such that the center portion of the fin 200 is unprotected. Then ions, preferably of the silicon or germanium with a normal dosage in the range of $1 \times 10^{14}\,cm^{-2}$ to $5 \times 10^{14}\,cm^{-2}$, are implanted into the center portion of the fin as indicated by item 700. The process of implanting ions into the center portion of the fin changes the center portion of the fin into an amorphous or polycrystalline semiconductor with a high density of mid-gap states.

[Para 43] The density of mid-gap states in the junction of a P-N diode strongly influences two important characteristics of the electrical conduction of such a diode, namely, the reverse-bias leakage, and the forward-bias ideality. The reverse-bias leakage is typically a very low current density (~1 $pA/cm^2$), however, when a high density of mid-gap states is introduced into the junction region, this reverse-bias current can increase many factors of ten. The forward-bias conduction current grows exponentially with forward voltage with an exponential factor of enkT/Qe, where k and Qe are Boltzmann's constant and the unit of electric charge, respectively, T is the temperature of the junction an n is a number, typically between 1 and 2, called the ideality factor. For low densities of mid-gap states n~1, while for large densities of mid-gap states, n~2.

[Para 44] The process of converting the end portions of the fin into N-type and P-type regions comprises a two-step process that protects one of the ends and the center portion of the fin while the other end is implanted with a doping impurity. More specifically, as shown in Figure 8, a mask 800 is

formed over one end of the fin 200 and over the center section of the fin 200, leaving only the other end of the fin exposed. Then an impurity 802 is implanted into the exposed end of the fin. Similarly, as shown in Figure 9, the first mask 800 is removed and a second mask 900 used to cover the previously exposed portion of the fin 200 and the center portion of the fins 200. Then, an opposite type of doping impurity 902 is implanted into the exposed portion of the fin. If desired, additional masking can be performed in this process. For example, an additional mask similar to the mask 500 shown in Figure 5, above, can be used in conjunction with this process. After the mask 900 is removed, the fin 200 will include a first type of impurity region 112 (e.g., P-type), a center highly resistive amorphous region 110, and opposite type doped impurity region 114 (e.g., N-type).

[Para 45] Thus, this process involves protecting the N-type end 114 and implanting P-type impurities 802 into the P-type end 112, and protecting the P-type end 112 and implanting N-type impurities 902 into the N-type end 114. These N-type impurities and the P-type impurities comprise opposite type impurities. For example, the N-type impurities 902 can comprise arsenic, phosphorus, etc. while the P-type impurities 802 can comprise boron, etc. As would be understood by one ordinarily skilled in the art in light of this disclosure, the actual impurities that are used can change depending upon the materials used in the antifuse. Indeed, any combination of substances can be used so long as those substances cause the fin to act in a biased manner such that current is encouraged to flow primarily in one direction. After the P-type and N-type impurities are implanted into the ends of the fin, the fin is heated sufficiently to activate the impurities, typically using anneals of 800 $^{o}$C to 1050 $^{o}$C for between 1s to 30s. As mentioned above, in order to activate the fuse, current is passed through the fin, which causes the fin to heat. A forward voltage of between 1 and 2 Volts is applied to the diode for 0.01s to 5s to achieve temperatures of between 500 $^{o}$C and 700 $^{o}$C, which are typically sufficient to accomplish the structural change to larger polycrystalline semiconductor grains and a lower average density of mid-gap states.

[Para 46] Therefore, after the antifuse is manufactured, it is utilized within a circuit to form a connection or perform a logical function. Figure 11 illustrates a simplified schematic diagram of the inventive antifuse 117 electrically connected by wiring to two items, item A 115 and item B 119. Items A and B can comprise any type of item, such as a voltage source, controller, transistor, capacitor, etc. In one example, it may be desirable to connect item A to item B. In this case, the antifuse 117 would comprise the embodiment shown in Figure 6 and sufficient current or voltage would be generated through the fin 200 to heat the center portion 600 fin to a sufficient temperature to change the center portion 600 to a conductor. This would make the antifuse a permanent conductor between items A and B. If item A were not to be connected to item B, the antifuse would not undergo the heating process.

[Para 47] Alternatively, the antifuse 117 could represent the antifuse shown in Figure 10 and item A could represent a logical device and item B could comprise a voltage source. In its unactivated state, the antifuse 117 would provide one type of characteristic, namely the reverse-bias conduction current would be 100 to 1000 times that of the heated (annealed) antifuse. Thus, before the center portion of said fin is heated, the center portion of said fin has a reverse-bias leakage that is more than 100 times higher than the reverse-bias leakage after the center portion of said fin is heated. Additionally, the electrical conduction in the regime of 50 mV to 350 mV forward bias, would be characterized by an ideality factor, n = 2, which could represent one logical value. If this logical value were to be changed to an opposite logical value, the antifuse could be activated as described above by heating. Then, after activation, the antifuse would provide the opposite type of characteristic, namely lower reverse-bias conduction (100 to 1000 times lower reverse-bias conduction) or a forward-bias ideality factor, n=1, thereby providing item A with a different logical answer when accessing the antifuse 117. In the case that the antifuse in 117 represents the antifuse shown in Figure 6, the high-resistance state would initially exist due to the amorphous region 600 and could represent on logical value. A voltage would be provided

on the antifuse where programming is desired, to heat the amorphous region 600, thereby converting the region 600 to a low-resistance (conductor) state, which could represent a second logical value.

[Para 48] With respect to the heating that occurs within the center portion of 600, 110 of the fin 200, a narrower center portion allows a lower voltage to be utilized when performing the heating operation. Therefore, the masks 400 that are utilized should be patterned to make the center portion 600, 110 of the fin 200 and small as possible along the length of the fin 200. This requirement is balanced against the need for the center portion of the fin 200 to remain a high-resistance region before the antifuse is activated. Therefore, while each design will have different parameters, the length of the center portion 600, 110 of the fin 200 should be minimized to the greatest extent possible to reduce the amount of voltage required to generate the necessary heating. Thus, in one example, the size (length) of the center portion of the fin is restricted such that, for example, the center portion comprises less than approximately 5 to 10 percent of the length of the fin.

[Para 49] The subsequent selective heating of the fin changes the center portion of the fin into polycrystalline silicon. The selective heating of the fin that activates the antifuse in the embodiment shown in Figure 6, changes the conductivity level of the center portion of the fin to be many times (e.g., 10 or more times) more conductive after being heated above the predetermined temperature when compared to the conductivity level of the center portion before heating. In the embodiment shown in Figure 10, the amorphization of the fin increases the mid-gap density of states of the center portion of the fin to be many times (e.g., 100 or more times) that found in the unamorphized fin. Heating of this amorphized region decreases the density of states to a value nearby that of the original unamorphized fin, in the range of $< 10^{17}cm^{-3}eV^{-1}$.

[Para 50] Figure 12 illustrates the methodology of the invention in flowchart form. More specifically, in item 120, the invention forms a material layer and then patterns the material layer into a fin in item 122. Next, the

invention converts the center portion of the fin into an amorphous material (124) and converts the end portions of the fin into conductors (126) for them embodiment shown in Figure 6, or dopes the end portions of the fin using opposite type dopants (128), for the embodiment shown in Figure 10. For the embodiment shown Figure 10, the structure is then annealed to drive the dopants into the central region of the fin in item 130. The process of converting the center portion of the fin into an amorphous material allows the subsequent selective heating process 132 to convert the amorphous center portion of the fin into a conductor. Thus, the invention provides a fin-type structure that can be selectively converted from a high-resistance region into a permanent low-resistance region, or conductor, using a simple heating process.

[Para 51] The invention presents a method of forming an antifuse and the resulting structure. The inventive method and structure produce antifuses that use fin technology. Therefore, the inventive antifuses are smaller than conventional fuses. Thus, the invention takes advantage of the fact that a fin of silicon is of very low mass (fractions of a picogram) and thus is easily heated electrically. The invention provides an inexpensive technique to make the antifuse change resistance by a large amount permanently after a pulse of heating current is passed through the fin. Because of the small area (mass) of the inventive structure, the operation of activating (blowing) the antifuse involves a simplified heating process that is performed by passing current through the antifuse. Therefore, not only does the invention produce smaller antifuses than are conventionally available, the invention also provides a method of activating the fuses that avoids the problems that can occur during conventional physical/optical antifuse activation.

[Para 52] Benefits which accrue include high-density and low-power encoding of data, reduced cost for repair/replacement of redundant elements, ability to self-heal or self-program elements on a chip in the field, and increased versatility for use of circuits. These inventive methods and structures may apply to logic, memory, including SRAM, DRAM, and NVRAM, as well as analog and other integrated circuits.

[Para 53] The foregoing description of the specific embodiments will so fully reveal the general nature of the invention that others can, by applying current knowledge, readily modify and/or adapt for various applications such specific embodiments without departing from the generic concept. Therefore, such adaptations and modifications should and are intended to be comprehended within the meaning and range of equivalents of the disclosed embodiments. It is to be understood that the phraseology or terminology employed herein is for the purpose of description and not of limitation. Therefore, while the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.